

CD4001BM/CD4001BC Quad 2-Input NOR Buffered B Series Gate

CD4011BM/CD4011BC Quad 2-Input NAND Buffered B Series Gate

General Description

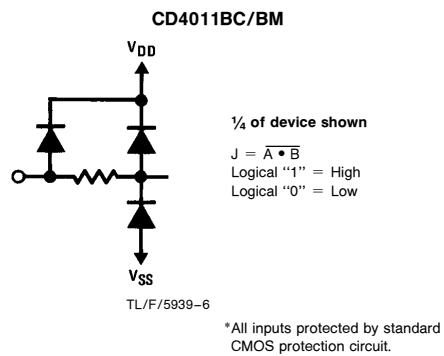
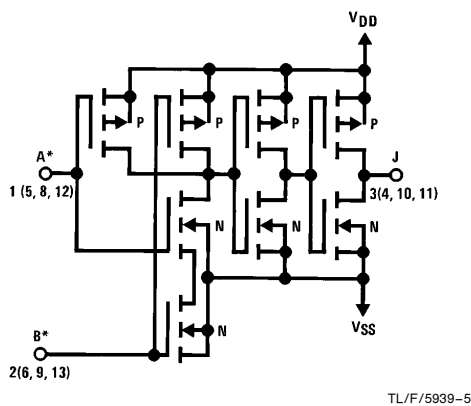
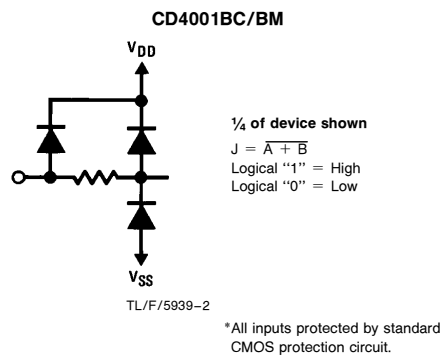
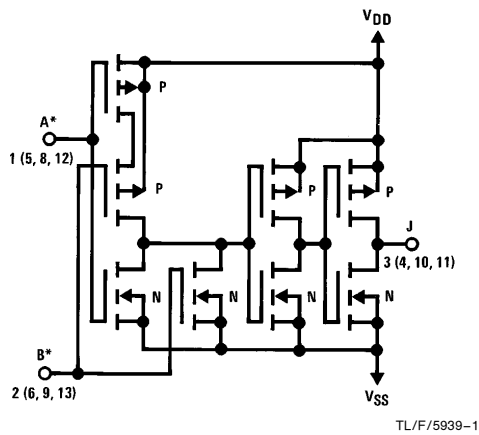
These quad gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain.

All inputs are protected against static discharge with diodes to V_{DD} and V_{SS} .

Features

- Low power TTL compatibility
 - 5V–10V–15V parametric ratings
 - Symmetrical output characteristics
 - Maximum input leakage 1 μ A at 15V over full temperature range
- Fan out of 2 driving 74L
or 1 driving 74LS

Schematic Diagrams



CD4001BM/CD4001BC Quad 2-Input NOR Buffered B Series Gate
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Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at any Pin	-0.5V to $V_{DD} + 0.5V$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
V_{DD} Range	-0.5 V_{DC} to +18 V_{DC}
Storage Temperature (T_S)	-65°C to +150°C
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Operating Conditions

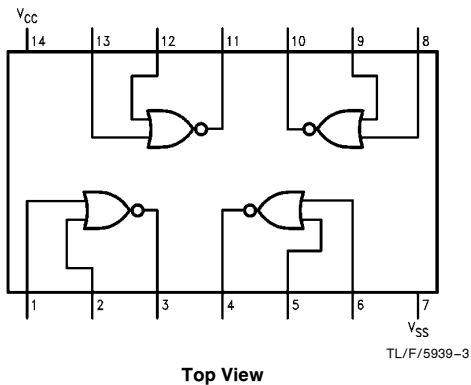
Operating Range (V_{DD})	3 V_{DC} to 15 V_{DC}
Operating Temperature Range	
CD4001BM, CD4011BM	-55°C to +125°C
CD4001BC, CD4011BC	-40°C to +85°C

DC Electrical Characteristics CD4001BM, CD4011BM (Note 2)

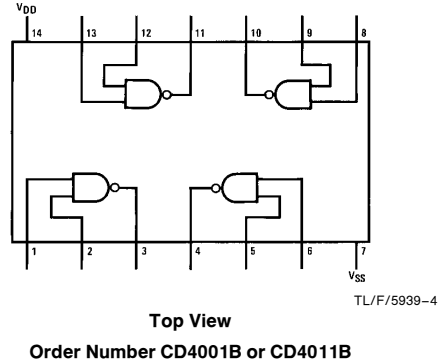
Symbol	Parameter	Conditions	-55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V, V_{IN} = V_{DD}$ or V_{SS} $V_{DD} = 10V, V_{IN} = V_{DD}$ or V_{SS} $V_{DD} = 15V, V_{IN} = V_{DD}$ or V_{SS}		0.25 0.50 1.0		0.004 0.005 0.006	0.25 0.50 1.0		7.5 15 30	μA μA μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$ } $ I_O < 1 \mu A$		0.05 0.05 0.05		0 0 0	0.05 0.05 0.05		0.05 0.05 0.05	V V V
V_{OH}	High Level Output Voltage	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$ } $ I_O < 1 \mu A$	4.95 9.95 14.95		4.95 9.95 14.95	5 10 15		4.95 9.95 14.95		V V V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V, V_O = 4.5V$ $V_{DD} = 10V, V_O = 9.0V$ $V_{DD} = 15V, V_O = 13.5V$		1.5 3.0 4.0		2 4 6	1.5 3.0 4.0		1.5 3.0 4.0	V V V
V_{IH}	High Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ $V_{DD} = 10V, V_O = 1.0V$ $V_{DD} = 15V, V_O = 1.5V$	3.5 7.0 11.0		3.5 7.0 11.0	3 6 9		3.5 7.0 11.0		V V V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$ $V_{DD} = 10V, V_O = 0.5V$ $V_{DD} = 15V, V_O = 1.5V$	0.64 1.6 4.2		0.51 1.3 3.4	0.88 2.25 8.8		0.36 0.9 2.4		mA mA mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 4.6V$ $V_{DD} = 10V, V_O = 9.5V$ $V_{DD} = 15V, V_O = 13.5V$	-0.64 -1.6 -4.2		-0.51 -1.3 -3.4	-0.88 -2.25 -8.8		-0.36 -0.9 -2.4		mA mA mA
I_{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$ $V_{DD} = 15V, V_{IN} = 15V$		-0.10 0.10		-10^{-5} 10^{-5}	-0.10 0.10		-1.0 1.0	μA μA

Connection Diagrams

CD4001BC/CD4001BM
Dual-In-Line Package



CD4011BC/CD4011BM
Dual-In-Line Package



DC Electrical Characteristics CD4001BC, CD4011BC (Note 2)

Symbol	Parameter	Conditions	-40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I _{DD}	Quiescent Device Current	V _{DD} = 5V, V _{IN} = V _{DD} or V _{SS}		1		0.004	1		7.5	μA
		V _{DD} = 10V, V _{IN} = V _{DD} or V _{SS}		2		0.005	2		15	μA
		V _{DD} = 15V, V _{IN} = V _{DD} or V _{SS}		4		0.006	4		30	μA
V _{OL}	Low Level Output Voltage	V _{DD} = 5V } I _O < 1 μA		0.05		0	0.05		0.05	V
		V _{DD} = 10V }		0.05		0	0.05		0.05	V
		V _{DD} = 15V }		0.05		0	0.05		0.05	V
V _{OH}	High Level Output Voltage	V _{DD} = 5V } I _O < 1 μA	4.95		4.95	5		4.95		V
		V _{DD} = 10V }	9.95		9.95	10		9.95		V
		V _{DD} = 15V }	14.95		14.95	15		14.95		V
V _{IL}	Low Level Input Voltage	V _{DD} = 5V, V _O = 4.5V		1.5		2	1.5		1.5	V
		V _{DD} = 10V, V _O = 9.0V		3.0		4	3.0		3.0	V
		V _{DD} = 15V, V _O = 13.5V		4.0		6	4.0		4.0	V
V _{IH}	High Level Input Voltage	V _{DD} = 5V, V _O = 0.5V	3.5		3.5	3		3.5		V
		V _{DD} = 10V, V _O = 1.0V	7.0		7.0	6		7.0		V
		V _{DD} = 15V, V _O = 1.5V	11.0		11.0	9		11.0		V
I _{OL}	Low Level Output Current (Note 3)	V _{DD} = 5V, V _O = 0.4V	0.52		0.44	0.88		0.36		mA
		V _{DD} = 10V, V _O = 0.5V	1.3		1.1	2.25		0.9		mA
		V _{DD} = 15V, V _O = 1.5V	3.6		3.0	8.8		2.4		mA
I _{OH}	High Level Output Current (Note 3)	V _{DD} = 5V, V _O = 4.6V	-0.52		-0.44	-0.88		-0.36		mA
		V _{DD} = 10V, V _O = 9.5V	-1.3		-1.1	-2.25		-0.9		mA
		V _{DD} = 15V, V _O = 13.5V	-3.6		-3.0	-8.8		-2.4		mA
I _{IN}	Input Current	V _{DD} = 15V, V _{IN} = 0V		-0.30		-10 ⁻⁵	-0.30		-1.0	μA
		V _{DD} = 15V, V _{IN} = 15V		0.30		10 ⁻⁵	0.30		1.0	μA

AC Electrical Characteristics* CD4001BC, CD4001BM

T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200k. Typical temperature coefficient is 0.3%/°C.

Symbol	Parameter	Conditions	Typ	Max	Units
t _{PHL}	Propagation Delay Time, High-to-Low Level	V _{DD} = 5V	120	250	ns
		V _{DD} = 10V	50	100	ns
		V _{DD} = 15V	35	70	ns
t _{PLH}	Propagation Delay Time, Low-to-High Level	V _{DD} = 5V	110	250	ns
		V _{DD} = 10V	50	100	ns
		V _{DD} = 15V	35	70	ns
t _{THL} , t _{TLH}	Transition Time	V _{DD} = 5V	90	200	ns
		V _{DD} = 10V	50	100	ns
		V _{DD} = 15V	40	80	ns
C _{IN}	Average Input Capacitance	Any Input	5	7.5	pF
C _{PD}	Power Dissipation Capacity	Any Gate	14		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

Note 3: I_{OL} and I_{OH} are tested one output at a time.

AC Electrical Characteristics* CD4011BC, CD4011BM

$T_A = 25^\circ\text{C}$, Input t_r ; $t_f = 20$ ns. $C_L = 50$ pF, $R_L = 200\text{k}$. Typical Temperature Coefficient is $0.3\%/^\circ\text{C}$.

Symbol	Parameter	Conditions	Typ	Max	Units
t_{PHL}	Propagation Delay, High-to-Low Level	$V_{DD} = 5\text{V}$	120	250	ns
		$V_{DD} = 10\text{V}$	50	100	ns
		$V_{DD} = 15\text{V}$	35	70	ns
t_{PLH}	Propagation Delay, Low-to-High Level	$V_{DD} = 5\text{V}$	85	250	ns
		$V_{DD} = 10\text{V}$	40	100	ns
		$V_{DD} = 15\text{V}$	30	70	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5\text{V}$	90	200	ns
		$V_{DD} = 10\text{V}$	50	100	ns
		$V_{DD} = 15\text{V}$	40	80	ns
C_{IN}	Average Input Capacitance	Any Input	5	7.5	pF
C_{PD}	Power Dissipation Capacity	Any Gate	14		pF

*AC Parameters are guaranteed by DC correlated testing.

Typical Performance Characteristics

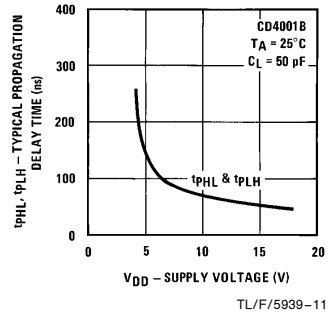
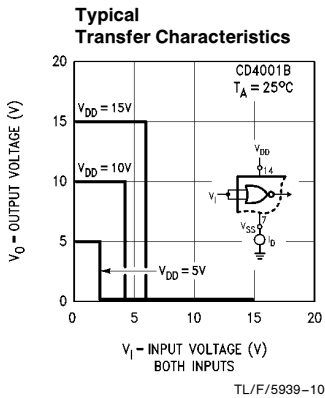
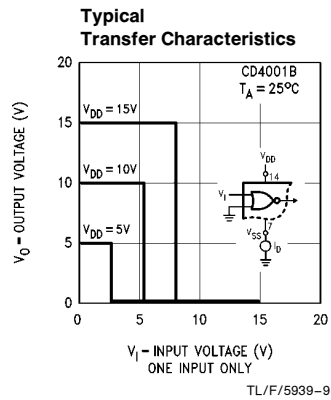
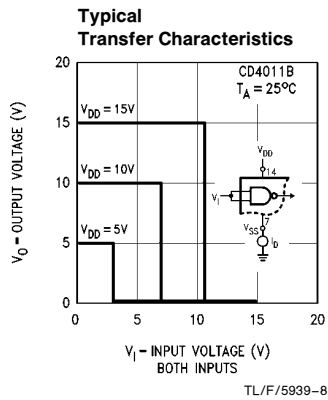
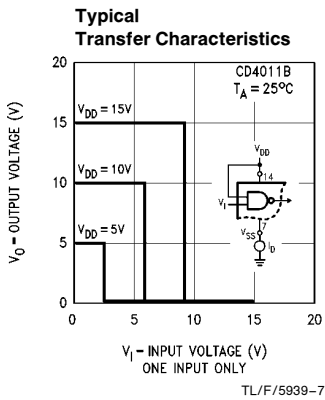


FIGURE 5

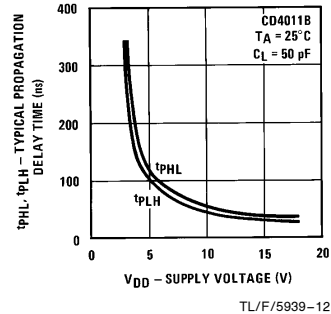


FIGURE 6

Typical Performance Characteristics (Continued)

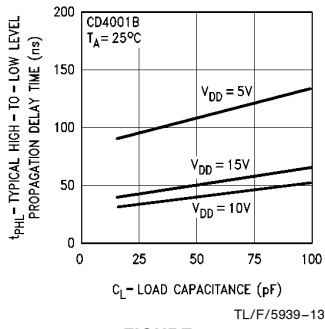


FIGURE 7

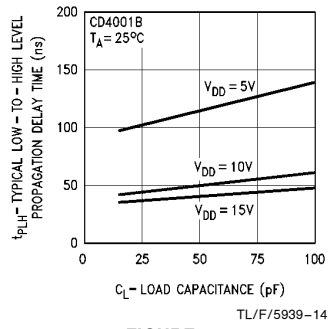


FIGURE 8

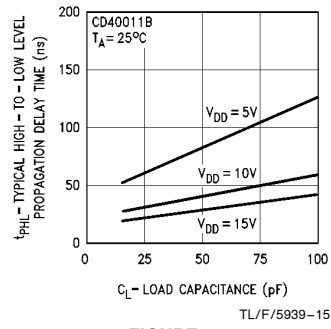


FIGURE 9

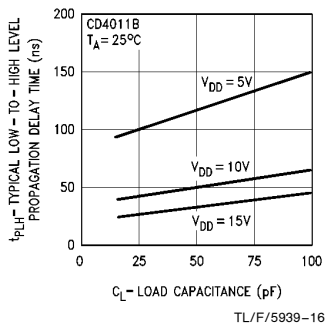


FIGURE 10

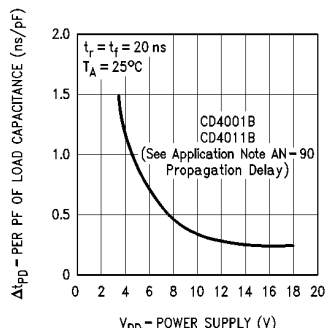


FIGURE 11

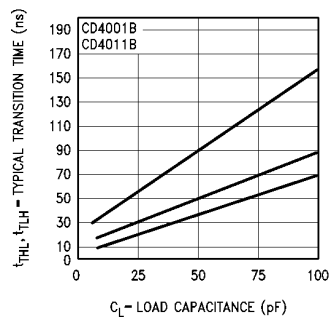


FIGURE 12

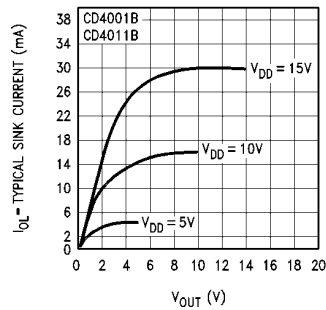


FIGURE 13

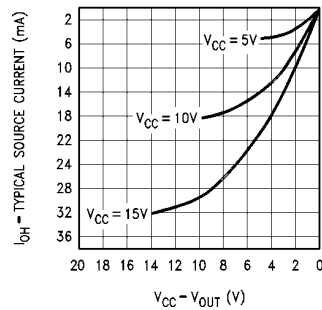
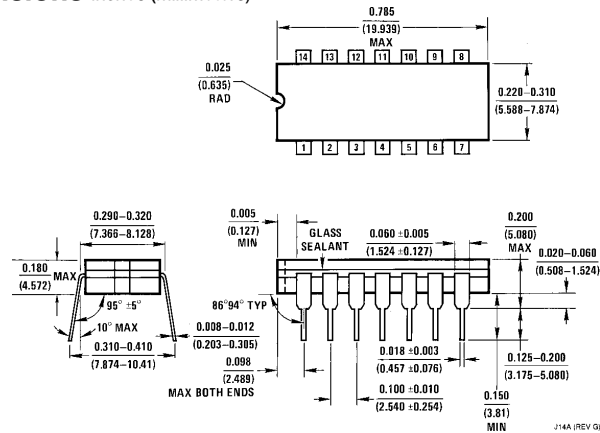


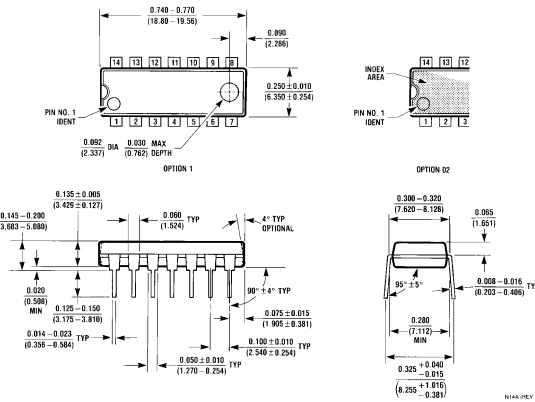
FIGURE 14

CD4001BM/CD4001BC Quad 2-Input NOR Buffered B Series Gate
CD4011BM/CD4011BC Quad 2-Input NAND Buffered B Series Gate

Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number CD4001BMJ, CD4001BCJ, CD40011BMJ or CD40011BCJ
NS Package Number J14A



Molded Dual-In-Line Package (N)
Order Number CD4001BMN, CD4001BCN, CD40011BMN or CD40011BCN
NS Package Number N14A

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